Amendments to the Specification

Please replace paragraph [0001] with the following amended paragraph:

[0001] ~~Not Applicable~~This application is a continuation of U.S. Application Serial No. 10/036,889, filed December 26, 2001, and entitled "Clock Skew Measurement Circuit on a Microprocessor Die".

Please replace paragraph [0015] with the following:

[0015] In the measurement unit, the reference clock signals and the target clock signals are compared. More particularly, the target clock signal is compared to each of the reference clock signals to determine whether that target clock signal makes a state transition before or after the particular reference clock signal. In this way, a determination is made regarding within which time window or bin the target clock signal makes its state transition. By running this comparison over several thousand clock cycles of the target clock signal, a pattern develops as to the outer boundaries of state transitions of the target clock.

Please replace paragraph [0048] with the following:

[0048] Each of the fine delay circuits 206, 208 is preferably an inverter. However, a logical inverter gate is merely a combination of transistors configured in such a way as to perform the inversion operation. Like any logic circuit, it takes a finite amount of time for a signal to propagate through the circuit. How fast a signal propagates through an inverter is proportional to the size of the transistors that make up that inverter gate. Where multiple transistors are operated in parallel, the speed at which the signal propagates through the logic gate is proportional to the cumulative size of the transistors that make up the logic gate. The preferred embodiment utilizes this fact in creating the programmable fine delay circuits 206, 208. In particular, each fine delay circuit 206 and 208 is an inverter implemented in such a way as to have a plurality of parallel transistors that may be selectively added or removed from the inverter circuit. In this way, the overall speed of each inverter 206, 208 may be adjusted. Such adjustable delay inverter circuits are known in the art~~, and for further information, reference is made to U.S. Patent No. _____ entitled~~

_____, ~~which disclosure is incorporated by reference herein as if reproduced in full below~~. Each of the fine delay control circuits 212, 214 are preferably responsible for digitally activating, when commanded, each set of parallel transistors as part of the overall delay setting.